IN THE CLAIMS:

Please amend claims 1-2, 18-21 and 25 as follows:

1. (Currently Amended) A semiconductor integrated circuit on a semiconductor chip, the semiconductor integrated circuit comprising:

a central processing unit conducting a single instruction multiple data (SIMD) command;

a single instruction multiple data (SIMD) unit controlled by the central processing unit and including a plurality of operation units conducting a concurrent operation for a plurality of data items respectively fetched therein in accordance with an interpretation result of said SIMD command by said central processing unit;

a data buffer connectible to said SIMD unit; and

a data transfer control unit for controlling transfer of data [[for]] between said data buffer and a memory,

wherein said data transfer control unit controls the transfer of data for a subsequent operation of said SIMD unit to said data buffer from [[a]] the memory in concurrence with the current operation of said SIMD unit for a plurality of data items read from said data buffer, and

wherein said data transfer control unit aligns the data for the subsequent operation from the memory, and the aligned data for the subsequent operation is transferred to the data buffer.

2. (Currently Amended) A semiconductor integrated circuit according to claim 1,

wherein said data buffer includes[[:]] a dual-port unit including a first port, and a second port,

said first port [[being]] is coupled via a first bus to said SIMD unit, and

said second port [[being]] is coupled via a second bus to said data transfer control unit.

3. (Previously Presented) A semiconductor integrated circuit according to claim 2, wherein said first port inputs or outputs said plurality of data items for said first bus, and

wherein said second port inputs or outputs said plurality of data items for said second bus.

4. (Previously Presented) A semiconductor integrated circuit according to claim 3, wherein said SIMD unit includes:

a first data register coupled to said first bus, said first data register being concurrently latched the plurality of data items; and

a second data register coupled to said first bus, said second data register being concurrently latched said plurality of data items,

wherein said plurality of operation units receive said plurality of data items respectively latched by said first and second data registers and for conducting said concurrent operation for said plurality of data items in said first and second data registers.

5. (Previously Presented) A semiconductor integrated circuit according to claim 2, wherein said central processing unit conducting operation control for said SIMD unit and access control via said first bus to said data buffer.

6. (Withdrawn) A semiconductor integrated circuit, comprising:

a single instruction multiple data (SIMD) unit conducting a concurrent operation for a plurality of data items;

a data buffer connected via a first bus to said SIMD unit; and

a data transfer control unit connected via a second bus to said data buffer, wherein

said data transfer control unit includes a bit extension unit for conducting bit extension for each of the plurality of data items transferred via said second bus to said data buffer.

7. (Withdrawn) A semiconductor integrated circuit according to claim 6, wherein said bit extension unit conducts 1-bit code extension according to a lower-most bit of the data.

8. (Withdrawn) A semiconductor integrated circuit according to claim 6, wherein said bit extension unit conducts bit extension for the plurality of data items in a concurrent fashion.

9. (Withdrawn) A semiconductor integrated circuit according to claim 6, further comprising a data aligner in a stage before said bit extension unit for the plurality of data items.

10. (Withdrawn) A semiconductor integrated circuit according to claim 6, wherein said data transfer control unit includes a bit removal unit for removing bits from each of the plurality of data items which are read from said data buffer and which are transferred via said second bus.

11. (Withdrawn) A semiconductor integrated circuit according to claim 10, wherein said bit removal unit removes a higher-most bit from the data.

12. (Withdrawn) A semiconductor integrated circuit according to claim 6, wherein said data buffer includes a dual-port unit including a first port and a second port,

said first port being connected via a first bus to said SIMD unit,

said second port being connected via a second bus to said data transfer control unit.

13. (Withdrawn) A semiconductor integrated circuit according to claim 12, wherein:

said first port concurrently input and output the plurality of data items for said first bus; and

said second port concurrently input and output the plurality of data items for said second bus.

14. (Withdrawn) A semiconductor integrated circuit according to claim 13, wherein said SIMD unit comprises:

a first data register connected to said first bus, said first data register being concurrently latched the plurality of data items;

a second data register connected to said first bus, said first data register being concurrently latched the plurality of data items; and

an operator for receiving the plurality of data items respectively latched by said first and second data registers and for conducting a concurrent operation for the data items.

15. (Withdrawn) A semiconductor integrated circuit according to claim 14, further comprising a central processing unit conducting operation control for said SIMD unit and access control via said first bus to said data buffer.

16. (Withdrawn) A semiconductor integrated circuit according to claim 15, wherein

said first and second data registers latch, in compression processing of image data, the image data;

said first data register latches, in expansion of image data, the image data; and

said second data register latches data of inverse discrete cosine transform (IDCT).

17. (Withdrawn) A semiconductor integrated circuit, comprising:

a single instruction multiple data (SIMD) unit conducting a concurrent operation for a plurality of data items;

a data buffer connectible to said SIMD unit;

a data transfer control unit for controlling transfer of data for said data buffer; and

a bit extension unit disposed on a data transfer path connecting said data buffer to said SIMD unit for conducting bit extension for each of the plurality of data items to said SIMD unit in a concurrent fashion.

18. (Currently Amended) A semiconductor integrated circuit according to claim 1, wherein said data transfer control unit includes a bit extension unit for conducting bit extension for each of said aligned data for the subsequent operation ~~plurality of data items~~ transferred via said second bus to said data buffer.

19. (Currently Amended) A semiconductor integrated circuit according to claim 18, wherein said bit extension unit conducts 1-bit code extension according to a lower-most bit of said aligned data ~~plurality of data items~~.

20. (Currently Amended) A semiconductor integrated circuit according to claim 18, wherein said bit extension unit conducts bit extension for said aligned data ~~plurality of data items~~ in a concurrent fashion.

21. (Currently Amended) A semiconductor integrated circuit according to claim 18, ~~further comprising~~ wherein the data transfer control unit includes a data aligner aligning for the data from the memory ~~in a stage before said bit extension unit for said plurality of data items~~.

22. (Previously Presented) A semiconductor integrated circuit according to claim 18, wherein said data transfer control unit includes a bit removal unit for removing bits from each of said plurality of data items which are read from said data buffer and which are transferred via said second bus.

23. (Previously Presented) A semiconductor integrated circuit according to claim 22, wherein said bit removal unit removes a higher-most bit from each of said plurality of data items.

24. (Previously Presented) A semiconductor integrated circuit according to claim 4, wherein said first and second data registers latch image data when being in compression processing of image data, and

wherein said first data register latches image data and said second data register latches data of inverse discrete cosiae transform (IDCT) when being in expansion of image data.

25. (Currently Amended) A semiconductor integrated circuit on a semiconductor chip, the semiconductor integrated circuit comprising:

a CPU executing a single instruction multiple data (SIMD) command;

a SIMD unit including operation units which concurrently execute operations of first data items fetched in the respective operation units in accordance with interpretation results of the [[SID]] SIMD command by the CPU;

a data buffer having:

a first port coupled to the operation units in the SIMD unit and providing the first data items to the operation units in the SIMD unit under control of the CPU, and

a second port;

a data transfer control unit coupled to the second port of the data buffer and controlling a transfer of the first data items to the second port of the data buffer, the data transfer control unit including:

first data aligners having inputs coupled to receive second data items from a memory and each having a bit shift function in 8 bits unit to a high-order side or a lower-order side to align the second data items for the operation units in the SIMD unit; and

bit extension units coupled to the second port of the data buffer and coupled to receive the aligned second data items and providing the first data items which are added ~~by adding~~ a sign bit to each of the aligned second data items,

wherein the data transfer control unit provides the next first data items to the data buffer unit for a subsequent operation of the SIMD unit, while executing the current first data items by the operation unit in the SIMD unit.

26. (Previously Presented) A semiconductor integrated circuit according to claim 25, wherein the data transfer control unit further comprises:

second data aligners having inputs coupled to the second port of the data buffer and each having a bit shift function in 8 bits unit to a high-order side or a lower-order side to align the third data items from the data buffer, the third data items being provided from the operation units in the unit as operation results of the first data items; and

bit removal units having inputs coupled to receive the aligned third data items and providing fourth data items to be provided to the memory by removing a sign bit from each of the third data items.